AMENDMENT TO THE CLAIMS

Please amend claims 1, 3 and 23 as follows:

1. (Currently Amended) A method of detecting a transition in an incoming signal ~~from a known previous logical state~~, comprising:

obtaining an oscillating reference;

receiving an incoming signal; and

comparing the oscillating reference against the incoming signal to detect a transition in the incoming signal relative to ~~the~~ a known previous logical state of the incoming signal.

2. (Original) The method of claim 1, wherein comparing includes generating a first result; and further comprising generating a control signal based on the previous logical state for controlling whether the first result drives an output signal.

3. (Currently Amended) The method of claim 2, wherein generating the control signal includes comparing the oscillating reference and the ~~output signal~~ previous logical state.

4. (Previously Amended) The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

5. (Original) The method of claim 3, wherein the first result drives the output signal from the previous logical state toward the first result; and generating a control signal includes comparing the oscillating reference and the output signal after the output signal logically equals the first result.

6. (Previously Amended) The method of claim 1, wherein the oscillating reference is received substantially synchronously with the incoming signal.

7. (Original) The method of claim 1, wherein the oscillating reference provides voltage and timing attributes.

8. (Original) The method of claim 1, wherein the oscillating reference is negated.

9. (Previously Amended) The method of claim 1, further comprising:

obtaining an oscillating reference complement; and comparing the complement against the incoming signal and against the previous logical state to detect a transition in the incoming signal relative to the previous logical state.

10. (Original) The method of claim 1, wherein the oscillating reference includes an oscillating source synchronous voltage and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

11. (Original) A system for detecting a transition in an incoming signal from a known previous logical state, comprising:

first and second input terminals for receiving, respectively, an oscillating reference and an incoming signal;

an output terminal providing an output signal logically equal to the previous logical state;

a first comparator coupled to the first and second input terminals for comparing the reference and the incoming signal to generate a first result; and

a first controller coupled to the first comparator for coupling the first result to the output terminal based on the previous logical state.

12. (Original) The system of claim 11, wherein the first controller compares the oscillating reference and the output signal.

13. (Original) The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare the oscillating reference and the output signal while the output signal is still logically equal to the previous logical state.

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14. (Previously Amended) The system of claim 12, wherein the first result is coupled to the output terminal to drive the output signal from the previous logical state toward the first result; and the first controller is coupled to compare the oscillating reference and the output signal after the output signal logically equals the first result.

15. (Previously Amended) The method of claim 11, wherein the oscillating reference is received substantially synchronously with the incoming signal.

16. (Original) The system of claim 11, wherein the oscillating reference provides voltage and timing attributes.

17. (Original) The system of claim 11, wherein the oscillating reference is negated.

18. (Original) The system of claim 11, wherein the oscillating reference includes an oscillating source synchronous voltage and timing reference having a slew rate and a cycle time, the slew rate being substantially equal to one-half the cycle time.

19. (Previously Amended) The system of claim 11, further comprising:

a third input terminal for receiving an oscillating reference complement;

a second comparator coupled to the second and third input terminals for comparing the complement and the incoming signal to generate a second result; and

a second controller coupled to the second comparator for coupling the second comparator to the output terminal based on the previous logical state.

20. (Previously Amended) A method of comparing an incoming signal to a previous logical state, comprising the steps of:

obtaining an oscillating reference and an oscillating reference complement, the oscillating reference complement being a complement of the oscillating reference;

receiving the incoming signal;

comparing by a first comparator the oscillating reference against the incoming signal to generate a first result;

comparing by a second comparator the oscillating reference complement against the incoming signal to generate a second result;

using a control signal based on the previous logical state to control whether the first result or the second result passes as an output signal.

21. (Original) The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically the same as the previous logical state; and the control signal allows the second result to pass as the output signal.

22. (Previously Amended) The method of claim 20, wherein the previous logical state previously drove the output signal via the first comparator; the incoming signal is logically opposite the previous logical state; and the control signal allows the first result to pass as the output signal.

23. (Currently Amended) A receiver comprising:

a first comparator for comparing an oscillating reference and a new signal;

a second comparator for comparing a complement of the oscillating reference and the new signal;

an output terminal coupled to one of the first and second ~~comparators~~ comparators; circuitry

~~circuitry~~ for maintaining the comparator that is coupled to the output terminal when the new signal transitions; and

circuitry for coupling to the output terminal one of the first and second comparators that is not coupled to the output terminal and de-coupling from the output terminal one of the first and second comparators that is coupled to the output terminal when the new signal does not transition.

24. (Original) The method of claim 1, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

25. (Previously Amended) The method of claim 24, wherein the small-swing signals swing approximately 0.5 volts.

26. (Original) The system of claim 11, wherein the known previous logical state is a full-rail voltage; and the oscillating reference and incoming signal are both small-swing signals.

27. (Previously Amended) The system of claim 26, wherein the small-swing signals swing approximately 0.5 volts.

28. (Original) The system of claim 1, wherein the oscillating reference comprises a ramp signal.

29. (Original) The system of claim 1, wherein the oscillating reference is a discontinuously varying signal.

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30. (Original) The method of claim 11, wherein the oscillating reference comprises a ramp signal.

31. (Original) The method of claim 11, wherein the oscillating reference is a discontinuously varying signal.

32. (Original) The method of claim 11, wherein the first controller includes an exclusive-OR (XOR) logic gate.

33. (Original) The method of claim 19, wherein the second controller includes an exclusive-OR (XOR) logic gate.